

# Synchro V99x8

Working sheet for synchronizing  
multiple V99x8 VDP

# Inside V99x8

- V counter, count lines from 0 to 261(NTSC) or 312 (PAL).
- H counter, count N horizontal clock per line.
- H frequency is  $XtalFreq/N$ .
- N change depending on S1,S0 of REG#9.
- For S1,S0 = 0  $\rightarrow$  N=1368 (MSX ONLY).
- For S1,S0 = 1 or 2  $\rightarrow$  N=1365 (SUPER IMPOSE/ MIX).

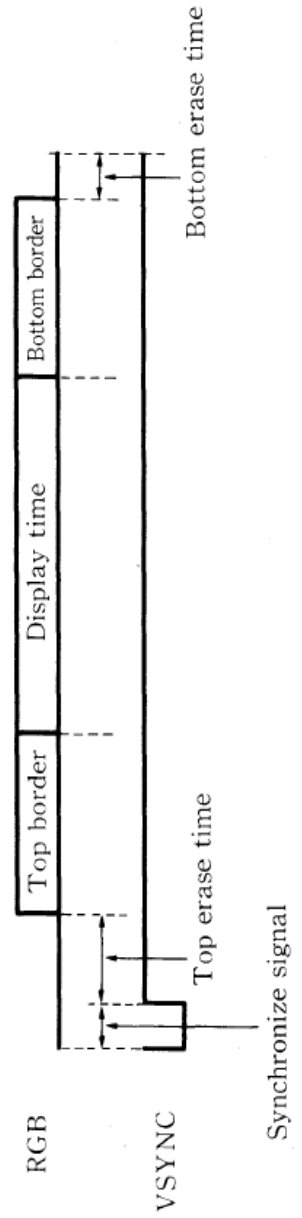
The three following slide show informations synthetized here

7-3 Vertical display parameters (PAL)

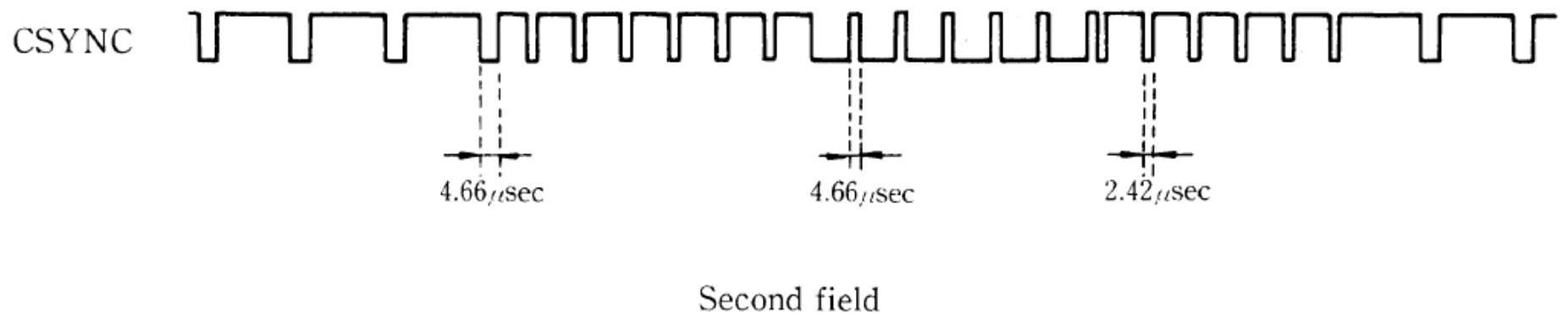
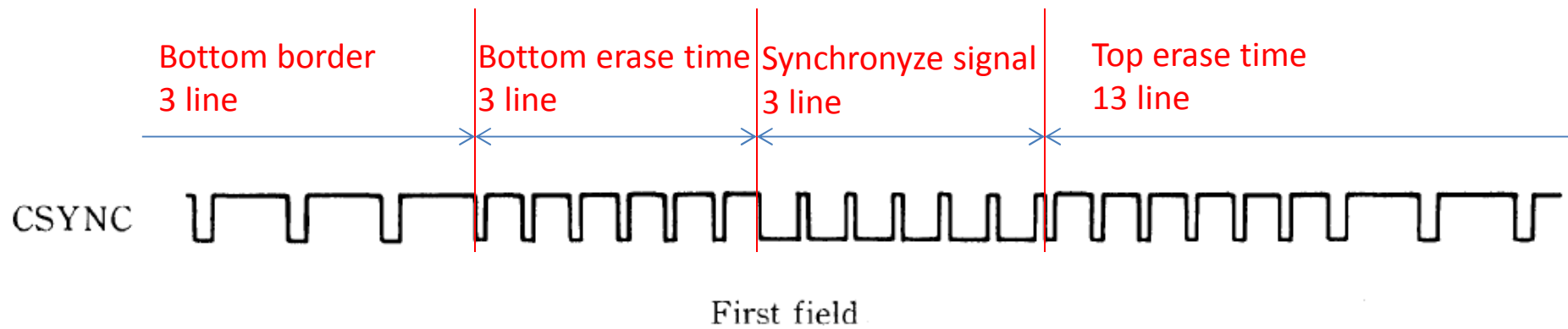
Unit: Lines

Lines	192 lines LN = 0			212 lines LN = 1		
	Non-Interlace	Interlace		Non-Interlace	Interlace	
		1st	2nd		1st	2nd
Synchronize signal	3	3	3	3	3	3
Top erase time	13	13.5	13	13	13.5	13.5
Top border	53	53	43	43	43	43
Display time	192	192	212	212	212	212
Bottom border	49	48.5	39	38.5	38	38
Bottom erase time	3	3	3	3	3	3
Total	313	312.5	312.5	313	312.5	312.5

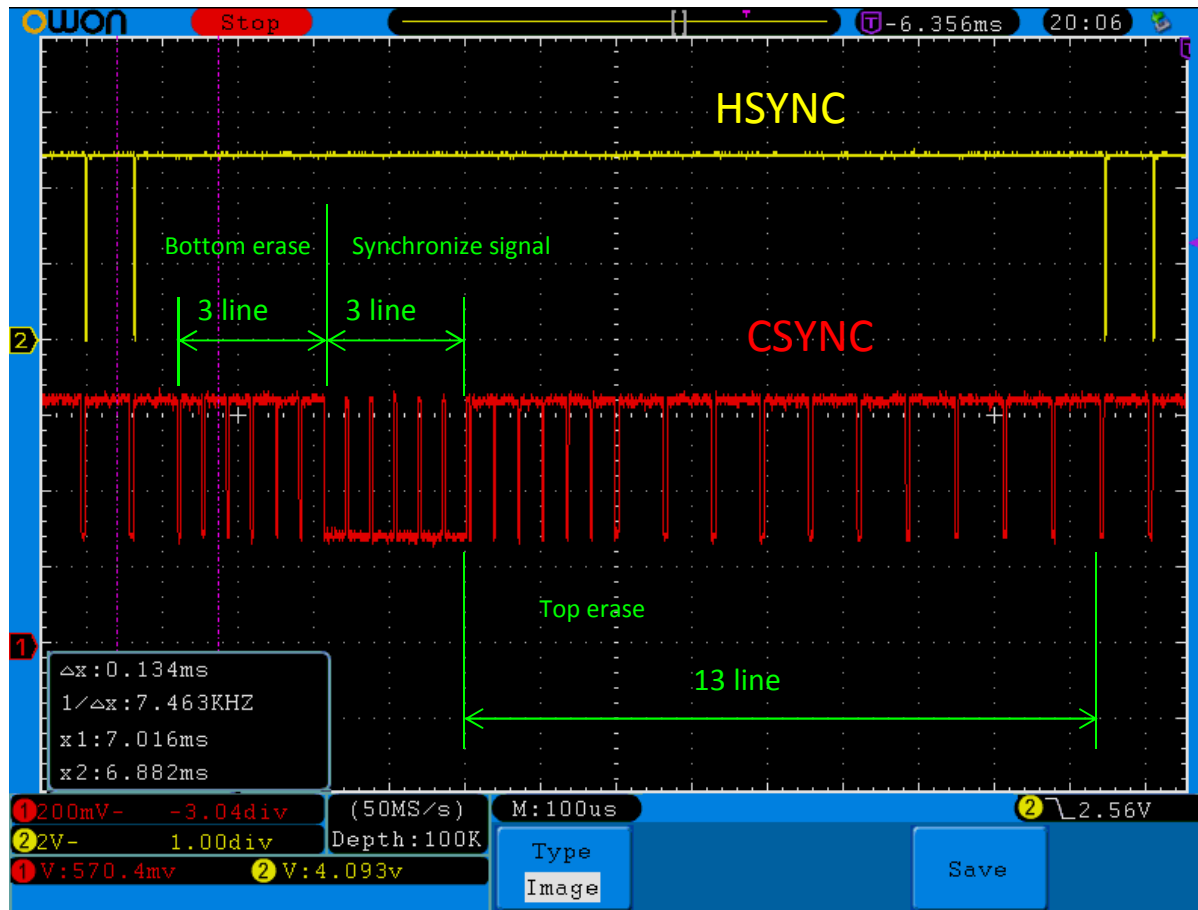
Note: The above table shows the relationship between RGB and VSYNC when the Display Adjust Register (Register Number 18) is set to 0.



After some data acquisition with a digital storage oscilloscope, you can see in red the position of the interesting part of the CSYNC signal. The oscilloscope snapshot is on next slide.



# Oscilloscope snapshot



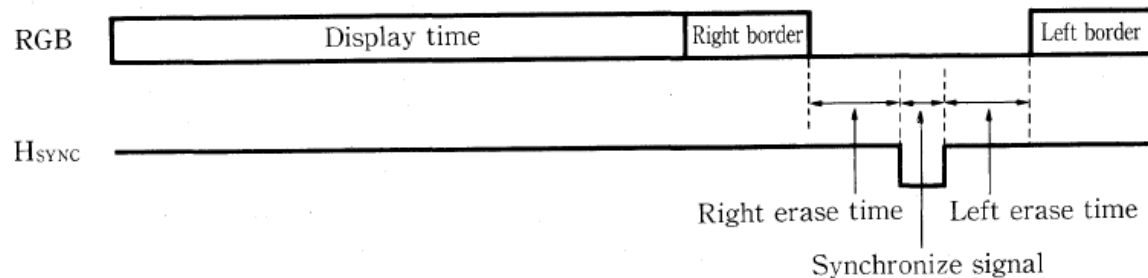
# Line timing (H counter)

## 7-1 Horizontal display parameters

Unit: XTAL Cycles

	Multicolor mode G1 to G7 modes		Text I mode Text II mode	
	Sl, S0 (R#9)	1, 2	0	1, 2
Display cycle	1024	1024	960	960
Right border	57	59	85	87
Right erase time	26	27	26	27
Synchronize signal	100	100	100	100
Left erase time	102	102	102	102
Left border	56	56	92	92
<b>Total</b>	<b>1365</b>	<b>1368</b>	<b>1365</b>	<b>1368</b>

Note: The above table shows the relationship between the RGB signal and HSYNC when the Display Adjust Register (Register Number 18) is set to 0.

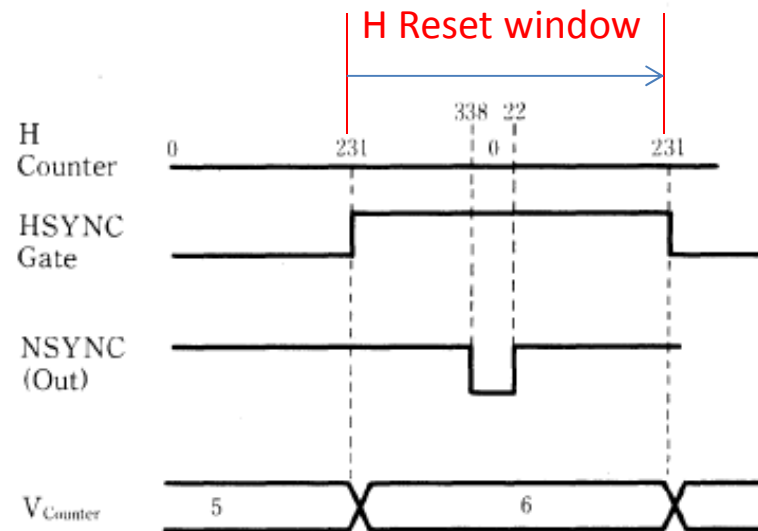


Synchronize input schem

## HSYNC input

When the V counter is set to 6, input from HSYNC is received, and the H counter is reset on the edge of the transition from High --> Low.

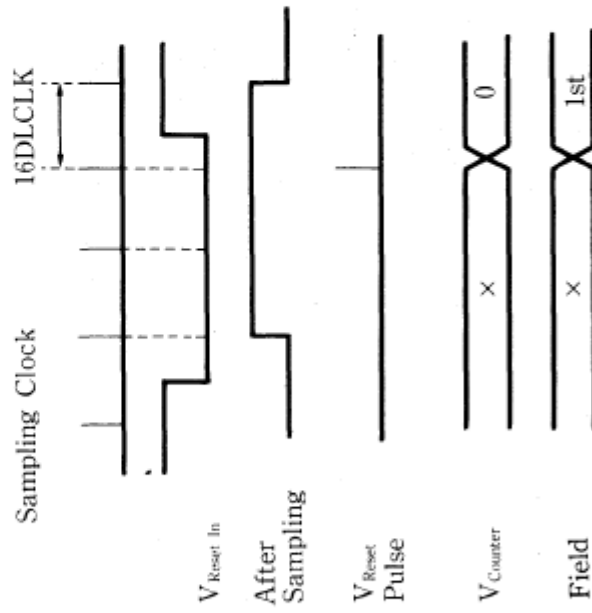
When the HSYNC Gate signal is Low, in other words, the V counter is set to a number other than 6, input signals to the HSYNC input are ignored.





### V Reset input (CSYNC)

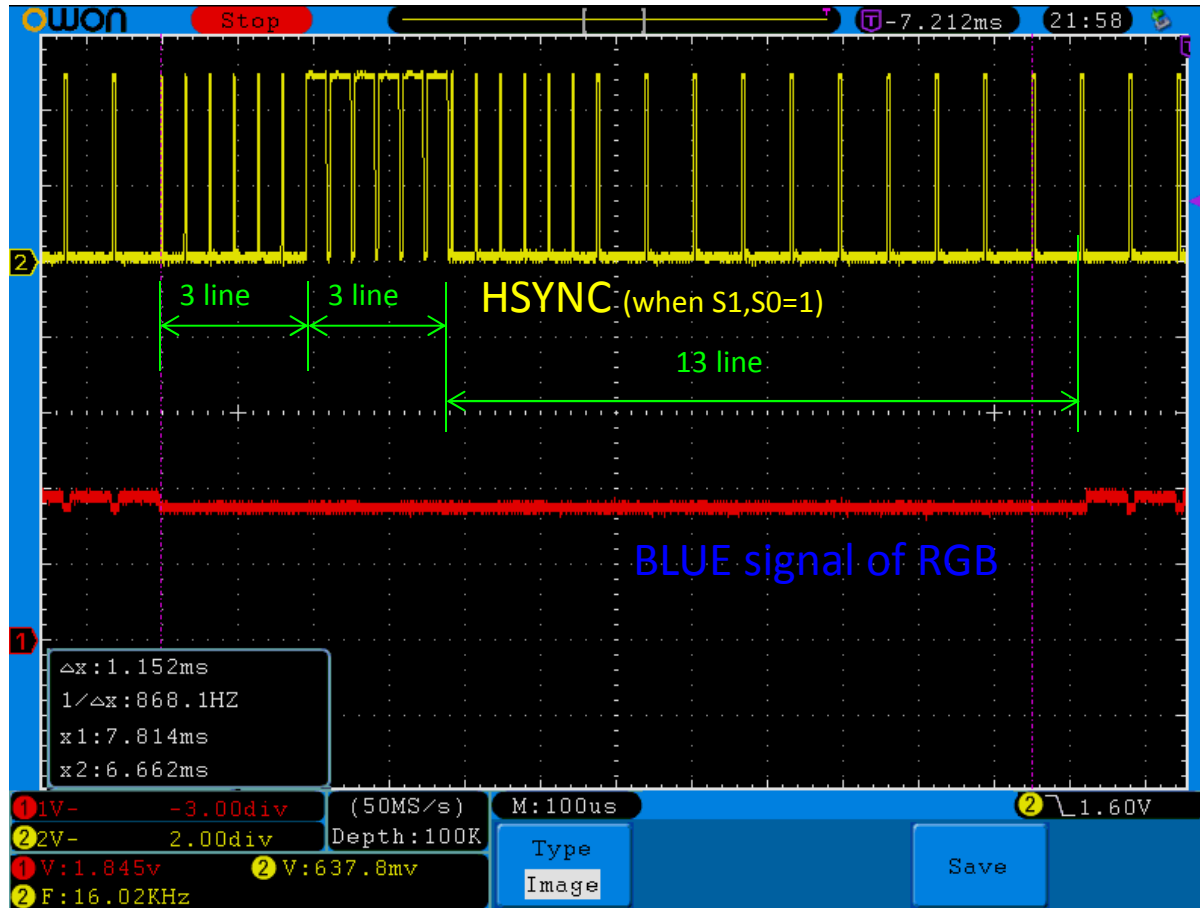
The V Reset signal is a signal that is internal to the V9938 that cycles at 2.98 us. When three consecutive Lows are received, the V counter is reset. Simultaneously, the first field is selected.



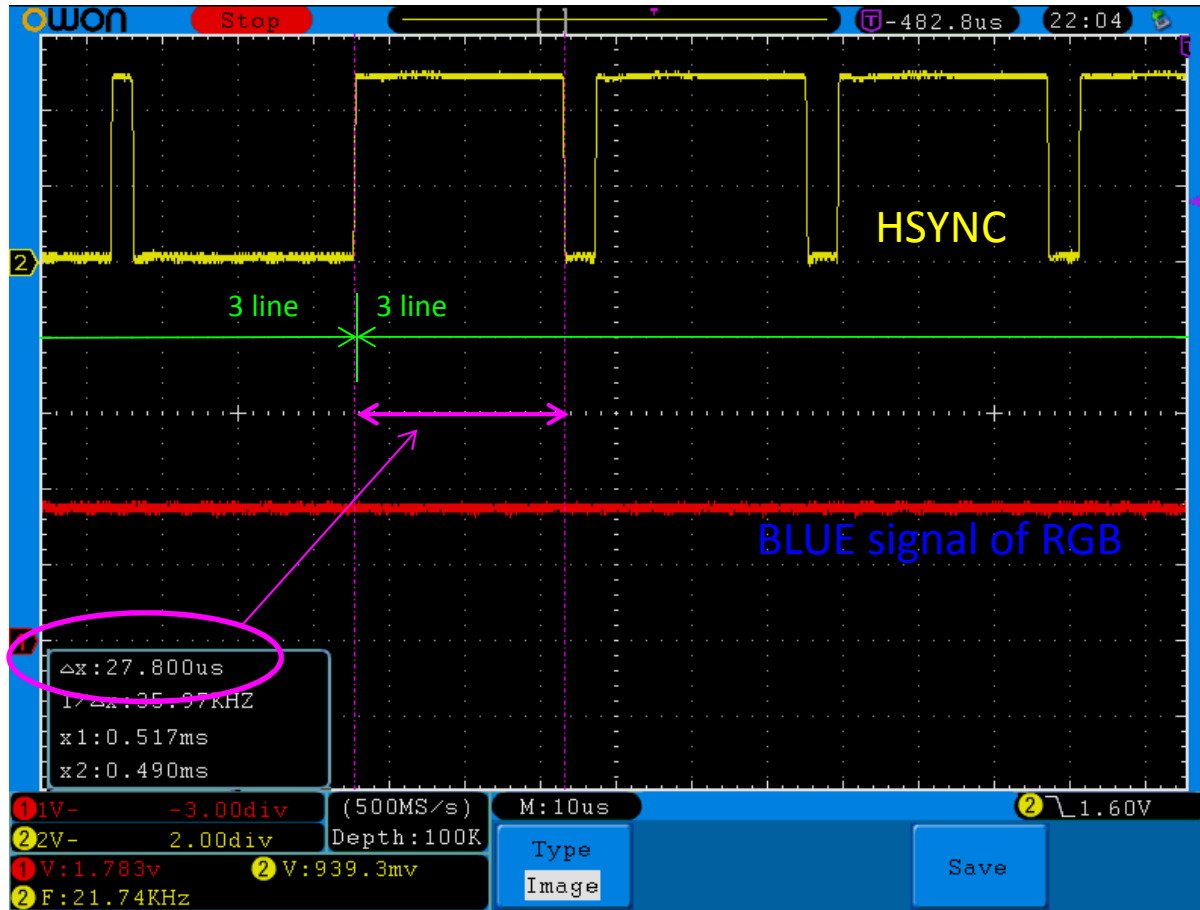
# My understanding

- Resetting V counter is possible at any time as long as you assert a reset signal of  $3 \times 2,98 \mu\text{s}$
- Resetting H counter only occurs when  $V=6$
- And  $H > 231$ ?

Configuration: 212 line PAL mode / S1,S0=1



Configuration: 212 line PAL mode / S1,S0=1



During blanking period the BLUE signal take the black level

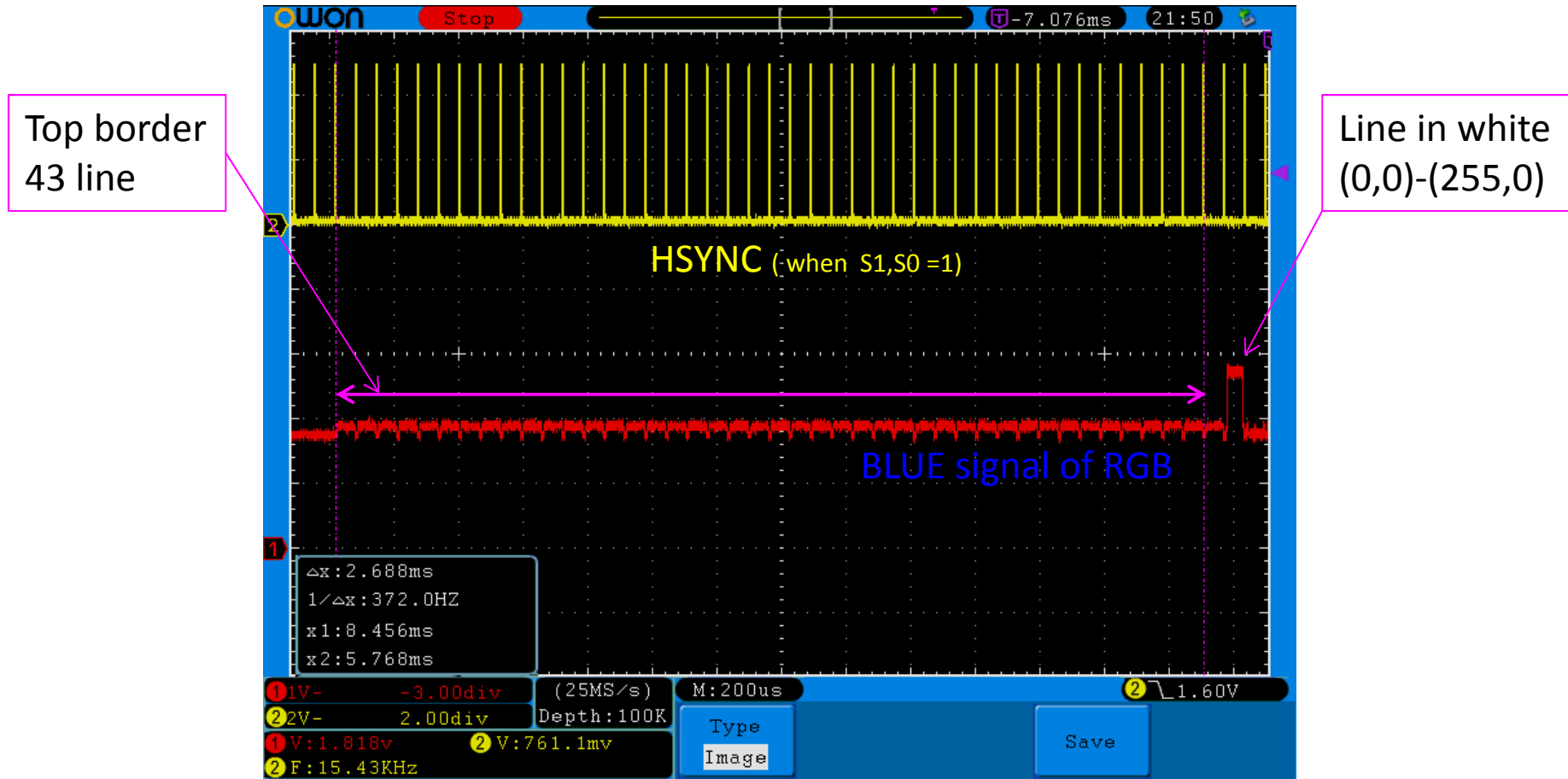
# Top border period

Test condition:

Boder color = 2

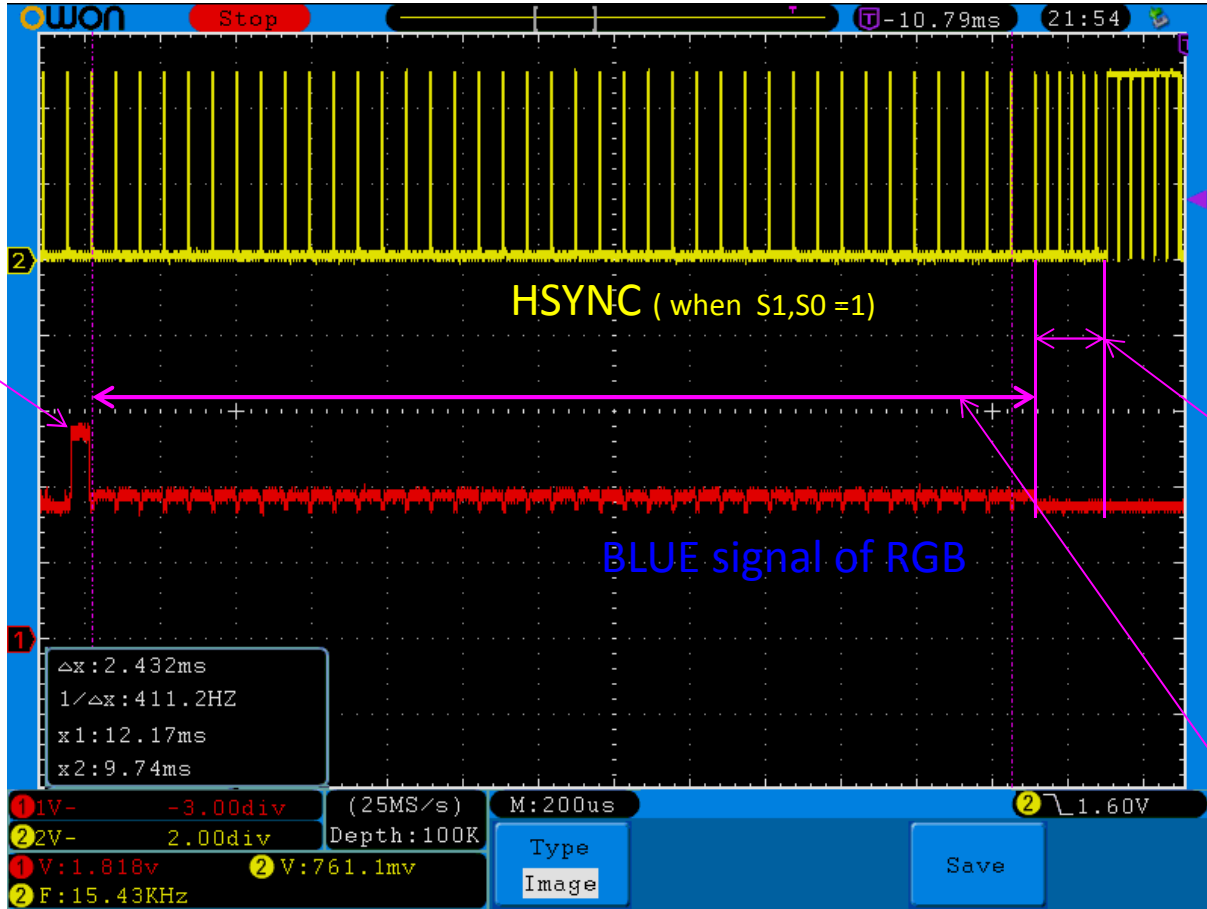
Line 0 and 211 are in color 15 (white)

Line 1 to 210 are in color 1 (black)



Configuration: 212 line PAL mode / S1,S0=1

Line in white  
(0,211)-(255,11)



Bottom erase  
time, 3 line

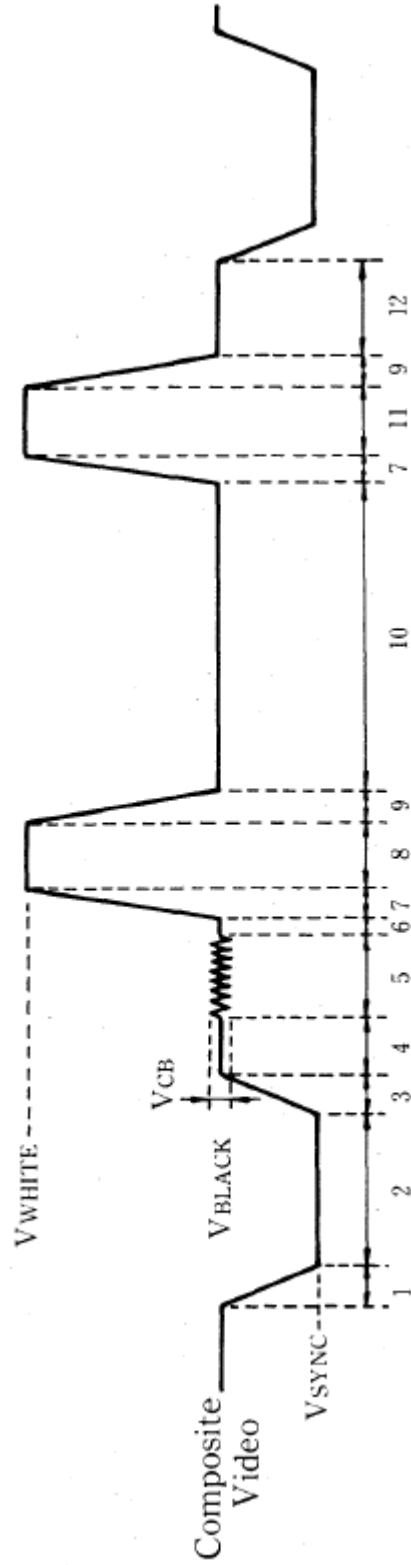
Top border  
39 line

Configuration: 212 line PAL mode / S1,S0=1

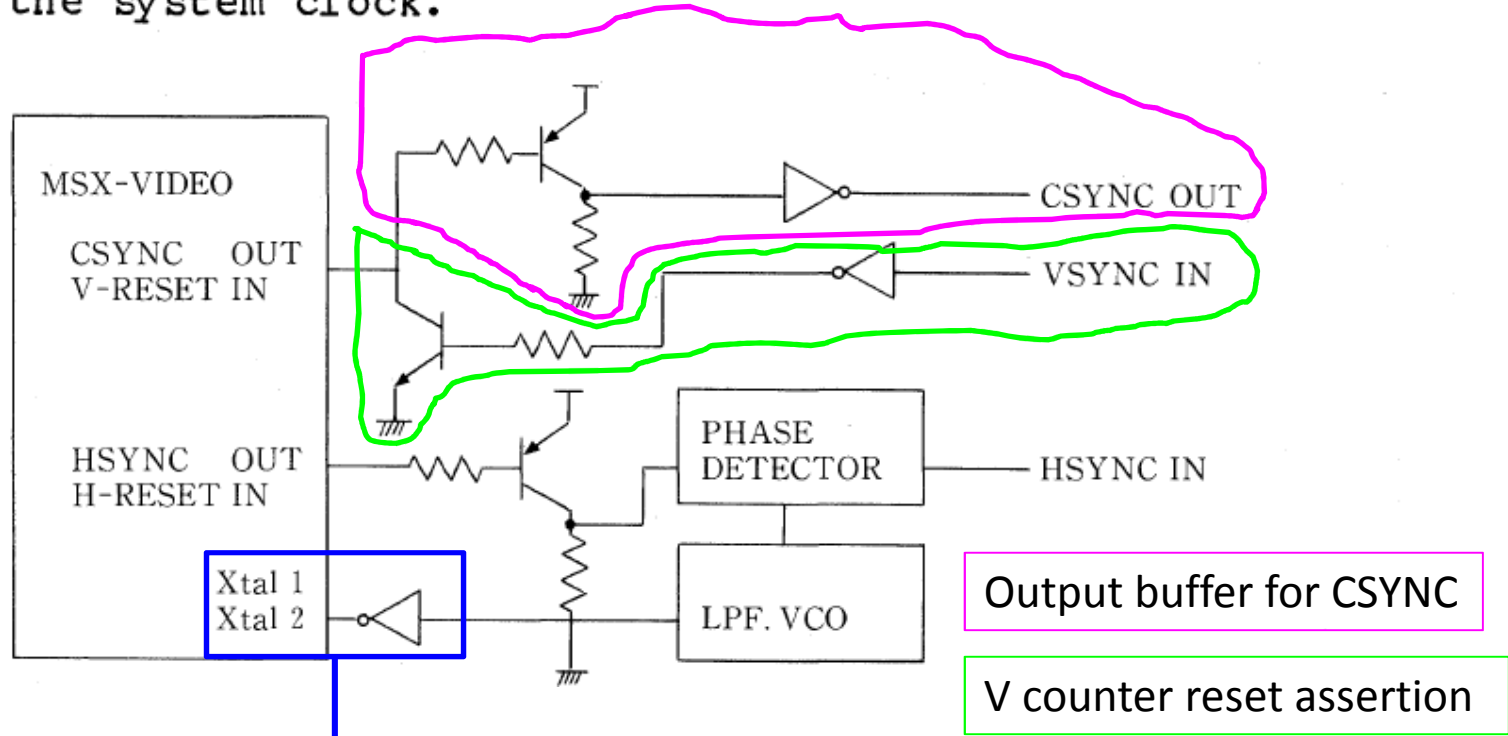
Composite video signal

No.	Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
1	TfCV 1	HSYNC fall time		4.50		110	ns
2	TWHS	HSYNC pulse width				4.70	us
3	TrCV 1	HSYNC rise time				90	ns
4	THS-CB	HSYNC color burst delay time		0.40		0.60	us
5	TWCB	Color burst width	RL = 470 ohms	2.60		3.30	us
6	TCB-LB	Color burst-left border delay time		1.10		1.50	us
7	TrCV 2	VBLACK-VWHITE rise time		2.4		90	ns
8	TwLB	Left border width	CL = 150 pF			2.7	us
9	TfCV 2	VWHITE-VBLACK fall time		47.00	47.68	100	ns
10	TWAD	Active display area		2.50		48.00	us
11	TrRB	Right border width				2.80	us
12	TRB-HS	Right border-horizontal synchronous delay time		1.20		1.50	us

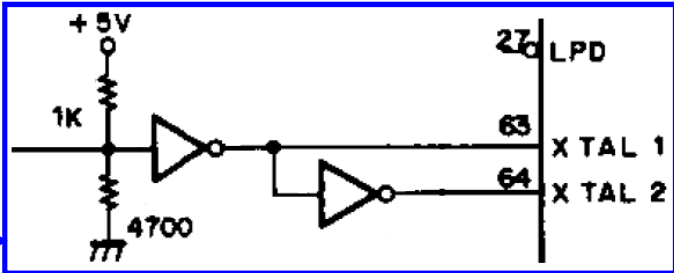
Note: Items 8 and 11 are when Display Adjust is 0.



The GENLOCK method detects the phase difference between the HSYNC output signal of the MSX-VIDEO and an external HSYNC signal and feeds it back to the system clock.

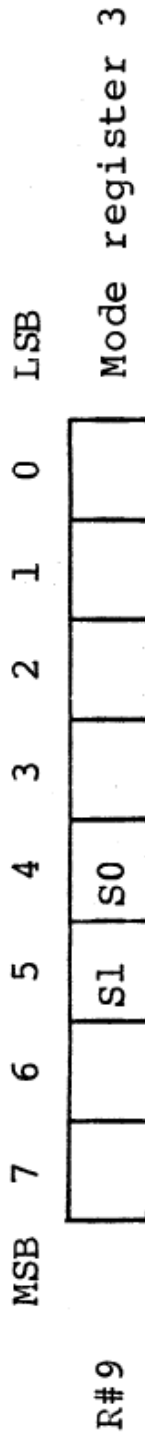


On V9958 Xtal1 is the input  
 On V9938 Xtal2 is the input  
 The SONY HB-900 is a better solution

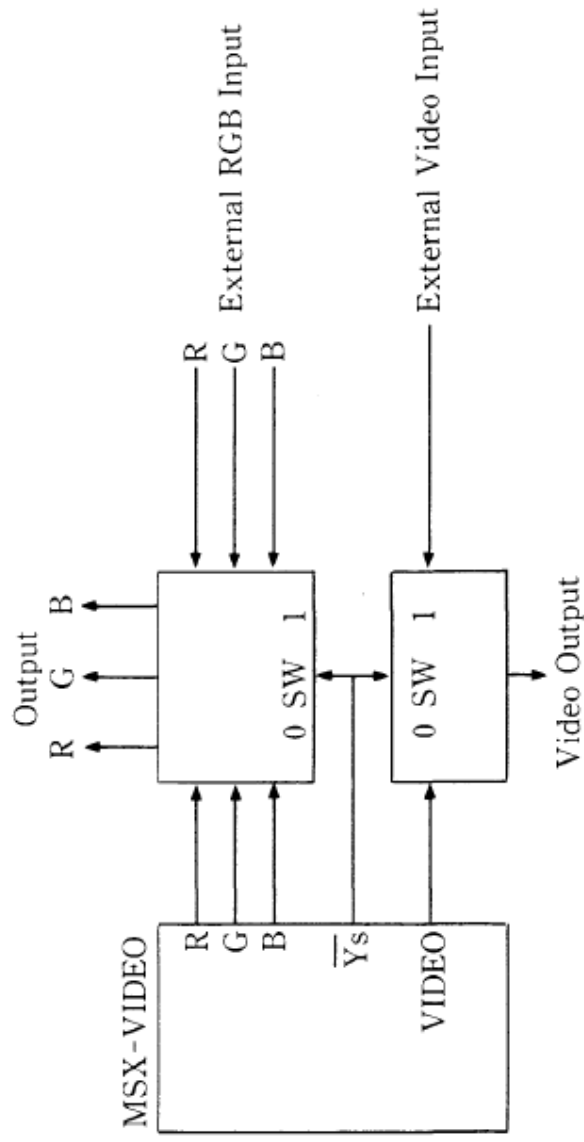




The S1 and S0 bits, bits 4 and 5 of register R#9, are used to set the synchronization mode of the MSX-VIDEO.



S1	IS0	Sync mode	*Ys	Purpose
0	0	PC SYNC	Selects Normal MSX-VIDEO (0)	Display the MSX-VIDEO screen
0	1	STD SYNC	Appears for transparent parts	Superimpose, digitize, etc.
1	0	STD SYNC	Selects external signal (1)	Display external screen
1	1	--	--	--



\*Ys selects the external video signal when scanning the transparent portion of the MSX-VIDEO screen.